

25 *C2*
26 *Concl'd*
27 forming a spacer insulating layer over said word line; and
28 forming a bit line above the top surface of said substrate so as to pass
29 over said word line but be insulated therefrom by said spacer insulating layer,
and so as to form an electrical contact with said drain region which is self aligned
with the edges of said space insulating layer.

REMARKS

Claims 1-5 are the original claims that went to the Board of Appeals but which have been amended herein to overcome the rejections of claims 2 and 3 for indefiniteness, which rejection was imposed in the final rejection Office Action dated 3/10/98. All prior art rejections of claims 1-5 have been overturned by the Board of Appeals. Claims 1-5 should now be in condition for allowance.

A new claim 6 directed to a method of making said EEPROM cell has been added.

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Respectfully submitted,

Ronald C. Fish

Ronald Craig Fish

Reg. No. 28,843

Tel 408 778 3624

FAX 408 776 0426

Ronfpatents@worldnet.att.net

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Ronald C. Fish

Ronald Craig Fish, President

Ronald Craig Fish a Law Corporation

Reg. No. 28,843

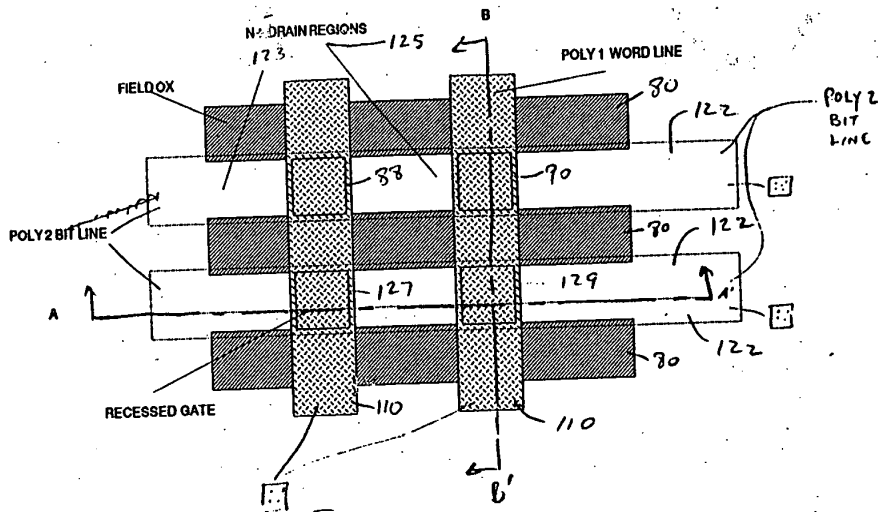


FIG. 32
TOP VIEW - FINISHED CELLS (FOUR)

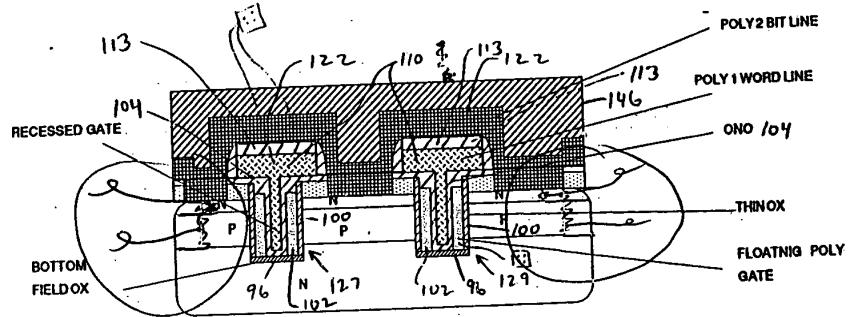


FIG. 33
SECTION A-A'

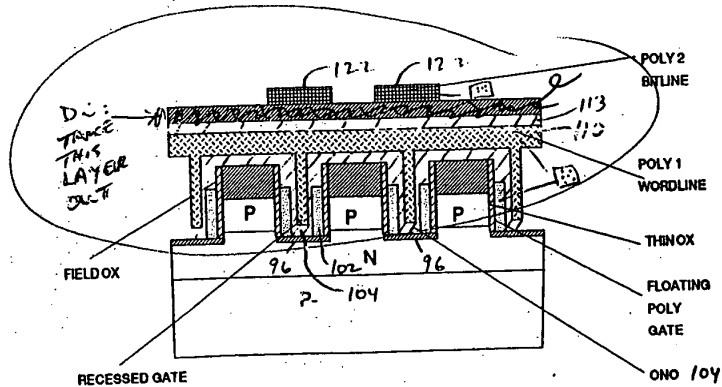


FIG. 34
SECTION B-B'

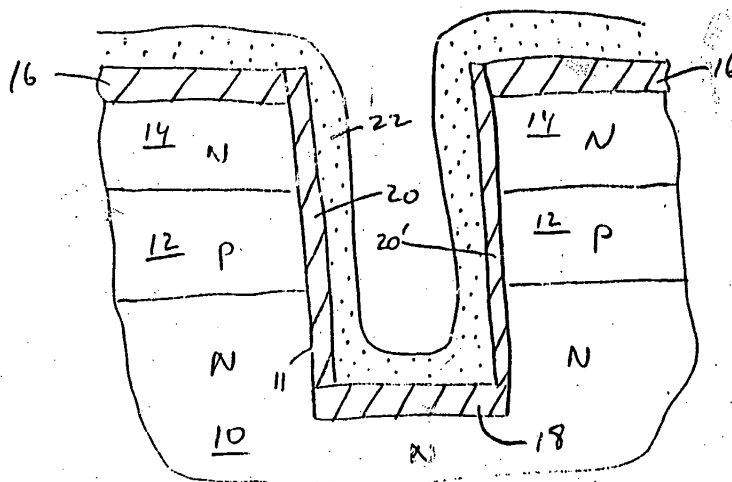


FIG. 1

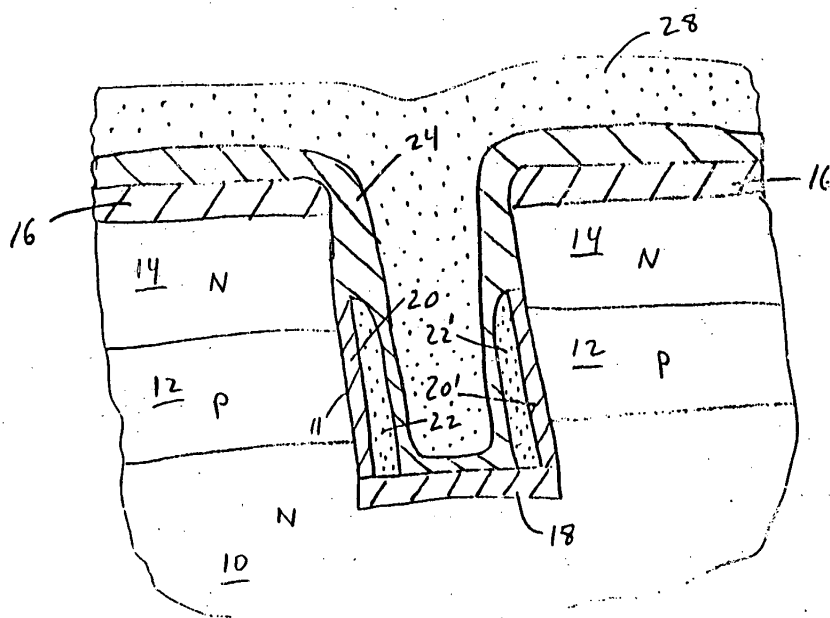


FIG. 2

